APPLICATION NOTE

Designing Low-cost, Multiple Output DC-DC Converters

Using 1:1 Coupled Inductors with Buck Regulators

1. Introduction

Power supply circuitry is always limited by cost, PCB area, height and by the desire to reduce complexity. The majority of systems today are mixed-signal, and in all but the simplest cases, the various analog and digital circuits need several different supply voltages to operate. One way to add additional outputs to a power supply without adding additional control ICs is to replace the standard inductor of a buck regulator with a multi-winding inductor. One winding is energized by the buck regulator, and there are many ways to create a second output by rectifying and filtering the voltage induced in the second winding. Buck regulators are found in nearly every power supply architecture, and the multi-winding inductor can be custom-wound to provide various turns ratios and even multiple outputs, but in the interest of controlling both complexity and cost, this application note will focus on off-the-shelf, 1:1 coupled inductors. Würth Elektronik eiSos offers several families of 1:1 coupled inductors with varying power levels and pinouts, many of which are suitable for adding a secondary output to a buck regulator.

2. The Three Most Common Used Topologies

Figures 1a, 1b and 1c show the three topologies that are most often used. Figure 1a shows how the secondary voltage, V_{OUT2} can be stacked on the main output voltage, V_{OUT1}, creating a total voltage with respect to system ground of (2 x V_{OUT1}).

Figure 1b shows how the return of the secondary output can be connected to the common of an isolated secondary, creating an isolated voltage that could be used to power sensors or isolated communications equipment. (Note: most 1:1 inductors are not rated to withstand the voltages in isolated AC mains or telecom circuits. Isolation with 1:1 inductors is used to insulate against electrical noise.) In this case, the average value of V_{OUT2} is equal to V_{OUT1}.

Figure 1c shows how the system ground can be shifted to the other side of the secondary output capacitor to create a negative voltage. In this case, the absolute value of V_{OUT2} is equal to V_{OUT1}.

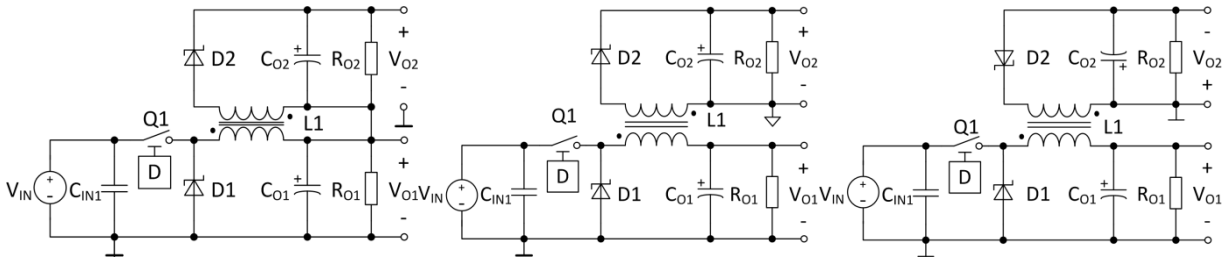

Figure 1a: Stacked for 2x VOUT **Figure 1b: Isolated VOUT2** **Figure 1c: Negative VOUT2**

In all three cases the control loop of the buck regulator only regulates V_{OUT1}, and hence the actual value of V_{OUT2} will vary with input voltage, with the voltage drops across the output diode in the secondary, with the load currents in both the main output and the secondary output and with duty cycle. For this reason a linear regulator is often used on the secondary to provide a truly regulated secondary output voltage.

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3. Design Example

The following equations and design philosophies will guide the user through the steps needed to add a secondary output to a non-synchronous buck regulator using a control IC with a fixed current limit. Most buck regulator ICs with internal power MOSFETs have a comparator that monitors the current flowing through the control or “high-side” MOSFET (Q1 in Figure 1), which is equal to the main inductor current when this MOSFET is on. Good quality ICs will specify a minimum threshold for this current limit over the full range of operating temperature, and in most cases when this limit is reached the IC will immediately turn the MOSFET off. As will be shown, this represents a maximum output power that must be shared between the main output and the secondary output. For the design example the IC used will be the TPS54160 from Texas Instruments. The Electrical Characteristics table of the datasheet states that the minimum current limit threshold over the full temperature range is 1,8A. The design specifications are as follows:

V_{IN} = 10 V to 14 V, nominal 12 V. Input ripple voltage Δv_{IN} = 0,2 V_{P-P}

V_{OUT1} = 5,0 V, I_{O1} = 400 mA to 500 mA, continuous. Output ripple Δv_{O1} = 60 mV_{P-P}

V_{OUT2} = 5 V (by definition), I_{O2-MAX} = 200 mA. Output ripple Δv_{O2} = 60 mV_{P-P}

Switching Frequency, f_{SW} = 500 kHz

Estimated Efficiency, η = 90 %

P_{OUT} = 3,5 W

The selection of the external components is the same regardless of how the secondary is connected; hence these calculations are valid for the cases shown in Figure 1a, 1b and 1c.

4. The 1:1 Inductor

Magnetics form the heart of any switching converter, from this example delivering 3,5 W to a multiphase full-bridge converter delivering kilowatts of power. For the 1:1 coupled buck the principal difference from a standard buck is the increase in peak-to-peak ripple current induced in the main (primary) winding. This is due to the additional energy stored and delivered to the secondary output, and the induced current changes the waveshape from a triangle wave to a trapezoid wave. Figure 2 shows the currents in the primary winding in pink and the secondary winding in green. The dot convention of the two windings is arranged so that the secondary winding conducts while the control MOSFET is off and the recirculating diode (D1) is on. In this way the average voltage over a switching cycle applied to the secondary is approximately equal to V_{OUT1}.

Figure 2: Primary (pink) and Secondary (green) Currents in the 1:1 Coupled Inductor

V_{IN} = 12,0 V, V_{O1} = 5,0 V, $V_{O2} \approx V_{O1}$, I_{O1} = 500 mA, I_{O2} = 100 mA

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It is important to distinguish between the average current and the DC current for the secondary. "Average Current", $I_{S\text{-}AVG}$, refers to the average height of the trapezoid waveform. "DC Current", $I_{O2\text{-}MAX}$, refers to the average current delivered to the load on the secondary. These two currents are not the same value, and much confusion can result from mixing them up. For clarity, the Average Current of a trapezoid waveform is equal to the DC Current divided by one minus the duty cycle. For the case of the secondary in a 1:1 coupled buck the maximum values are of interest for worst case calculations:

$$D_{MAX} = \frac{V_{OUT1} + V_{D1}}{V_{IN-MIN} + V_{D1}} = \frac{5 + 0{,}5}{10 + 0{,}5} = 0{,}54 \quad \textbf{EQ.1}$$

$$I_{A-AVG} = \frac{I_{O2-MAX}}{1 - D_{MAX}} = \frac{0{,}2A}{0{,}46} = 0{,}43A \quad \textbf{EQ.2}$$

V_{D1} is the typical forward voltage of the recirculating diode, D1

The inductance per winding is selected in the same way as with a standard buck, and is based upon the control of the peak-peak ripple current in the primary winding, denoted $\Delta ip\text{-}_{TRI}$:

$$D_{MIN} = \frac{V_{OUT1} + V_{D1}}{V_{IN-MAX} + V_{D1}} = \frac{5 + 0{,}5}{14 + 0{,}5} = 0{,}39 \quad \textbf{EQ.3}$$

$$L_{MIN} = D_{MIN} \frac{V_{IN-MAX} - V_{OUT1}}{\Delta i_{P-TRI} \times f_{SW}} \quad \textbf{EQ.4}$$

5. Inductor Ripple Current

One of the most important decisions to be made in designing the converter is how much ripple to allow. In normal buck converters the peak-peak ripple is usually set at 20 % to 40 % of the maximum DC output current. The range of 20 % to 40 % represents a good compromise, tested and confirmed by the design of countless switching converters, and gives a balance between size (larger ripple requires less inductance and therefore smaller inductors) and efficiency/noise (smaller ripple leads to lower RMS currents and lower EMI).

EQ.4 selects the inductance for the purely triangular portion of the primary ripple current, but the total ripple current, Δi_P, is equal to the sums of primary triangular and the total secondary ripple currents. Due to this additional ripple, the recommended range for $\Delta i_{P\text{-}TRI}$ is lower - from 10 % to 30 % of the maximum output current of the primary, $I_{O1\text{-}MAX}$. For this example $\Delta i_{P\text{-}TRI}$ = 30 % = 0,15 A:

$$L_{MIN} = 0.39 \frac{14V - 5V}{0.15A \times 500kHz} = 45{,}5\mu H$$

The next highest standard value of inductance is 47 µH, and this value, denoted L1, will be used henceforth. The triangular portion of primary ripple current is then:

$$\Delta i_{P-TRI} = D_{MIN} \frac{V_{IN-MAX} - V_{OUT1}}{L1 \times f_{SW}} = 0.39 \frac{14V - 5V}{47\mu H \times 500kHz} = 0{,}146A_{P-P}$$

Calculating the ripple current in the secondary is unfortunately much less straightforward. This quantity is highly dependent upon the leakage inductance of the 1:1 inductor, the load current, the forward voltage drop of the output diode, and the DC resistance (DCR) of the inductor windings (Figure 3).

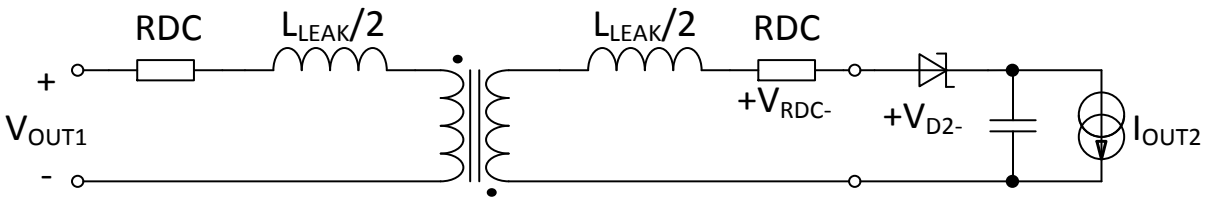

Figure 3: 1:1 Inductor with 1st Order Parasitic Components and Voltage Drops

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Closer inspection, especially at higher secondary output currents reveals that Δi_S is not purely triangular, but is in fact a parabola due to the trapezoid waveform of the voltage applied across the leakage inductance. An approximate equation is given here, based upon the assumption that the average voltage across the leakage inductance is constant and is equal to the forward voltage of the output diode:

$$\Delta i_S = \frac{2 \times V_{D2}}{L_{LEAK} \times f_{SW}}(1 - D_{MIN}) = \Delta i_S = \frac{2 \times 0{,}5V}{3{,}1\mu H \times 500kHz}(0{,}62) = 0{,}40A_{P-P} \quad \textbf{EQ.5}$$

The difficulty in using this expression stems from accurately measuring the leakage inductance and from accurately predicting (or measuring) the diode voltage V_{D2}. Leakage inductance is not always specified by inductor manufacturers, but it can be measured by short-circuiting one set of terminals of the inductor and measuring the inductance of the other terminals. For this example L_{LEAK} was measured as 3,1 µH. Diode voltage must be assumed, hence a value of 0,5 V will be used. With Δi_S estimated the total primary ripple current can be calculated:

$$\Delta i_P = \Delta i_{P-TRI} + \Delta i_S = 0{,}146A + 0{,}40 = 0{,}55A_{P-P} \quad \textbf{EQ.6}$$

Peak current can now be calculated for the primary:

$$I_{P-PEAK} = I_{O1-MAX} + \frac{\Delta i_P}{2} = 0.5A + \frac{0{,}55A}{2} = 0{,}77A \quad \textbf{EQ.7}$$

Peak current can be calculated for the secondary after the peak-peak secondary ripple current has been calculated:

$$I_{S-PEAK} = I_{S-AVG} + \frac{\Delta i_S}{2} = 0{,}42A + \frac{0{,}40A}{2} = 0{,}62A \quad \textbf{EQ.8}$$

The final step required before an actual inductor can be selected is to calculate the RMS currents for both the primary and the secondary. For the primary, using the DC output current is quick and very close to the true RMS value. For the secondary, the RMS value of a trapezoid wave is:

$$I_{S-RMS} = I_{S-AVG}\sqrt{1 - D_{MAX}}\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_S}{I_{S-AVG}}\right)^2} = 0{,}33A_{RMS} \quad \textbf{EQ.9}$$

6. The Right Inductor

In conclusion, the desired inductor should have an inductance of 47 µH per winding, be able to support a peak current of 0,77 A without saturating, and able to carry RMS currents of 0,5 A in one winding and 0,33 A in the other without overheating. With 1:1 coupled inductors it is especially important to read the datasheets carefully and to understand the conditions under which the saturation and RMS current ratings are valid. Good quality manufacturers will state these conditions explicitly. The Würth Elektronik WE-DD series of coupled inductors includes the 744 878 470, whose electrical characteristics are repeated below:

Order Code	L (µH)	I_R (A)	I_{SAT} (A)	R_{DC-TYP} (Ω)
744878470	47	0,9	1	0,6

I_R 40ºK over ambient temperature when **both** windings in series are energized by rated current mentioned. I_{SAT} inductance drop of 10% typical when **one** winding by saturation current mentioned

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The I_{SAT} rating is for the combination of the currents in both windings, however one fortunate aspect of 1:1 coupled bucks is that when current in one winding is at its peak, current in the other winding is at its valley, and hence the primary peak current I_{P-PEAK} represents the worst case.

7. Limits for Maximum Secondary Current

Two conditions limit the maximum current that the secondary output of a 1:1 coupled buck can deliver. The first is derived from the current limit threshold of the control IC. For this example where I_{LIM} = 1,8 A:

$$I_{O2-LIMIT} = (1-D_{MIN})(2\times I_{LIM} - 2\times I_{O1-MAX} - \Delta i_{P-TRI}) = 0.62\times(3{,}6A - 1{,}0A - 0{,}146A) = 1{,}52A \quad \textbf{EQ.10}$$

This condition is most likely to occur when both outputs are delivering maximum load current and when input voltage is at a maximum.

The second limitation comes from the boundary between Continuous Conduction Mode (CCM), where the current in the primary winding never reaches zero, and Discontinuous Conduction Mode (DCM), where primary current falls to zero before the end of the switching cycle. This limitation applies to non-synchronous buck converters and some synchronous buck converters if their control ICs do not allow inductor current to reverse polarity. Once the converter enters DCM the average voltage across the primary winding is less than V_{OUT1}. V_{OUT2} tends to droop or even collapse, depending upon the load current it supplies. For all switching regulators the CCM/DCM boundary can be defined as the point when average inductor current equals one-half of the ripple current. Referring back to Figure 2, it is clear that this condition is most likely to occur when primary load current is low and secondary load current is high.

Writing a useful equation is difficult because of the high variability of the secondary ripple current and its dependence upon the non-linear relationship of the secondary output diode forward voltage to forward current. Lab testing is the best way to determine when the converter will enter DCM, and a current probe will show the exact point where primary current hits zero. If a current probe is not available, then a voltage probe and a multimeter will work. Figure 4 shows the switch-node voltage of the primary (where the control FET, inductor primary and diode all connect) just in DCM. The voltage probe will reveal the onset of a damped oscillation before the end of each switching cycle, and a multimeter will show the rapid drop in V_{O2} once DCM is reached.

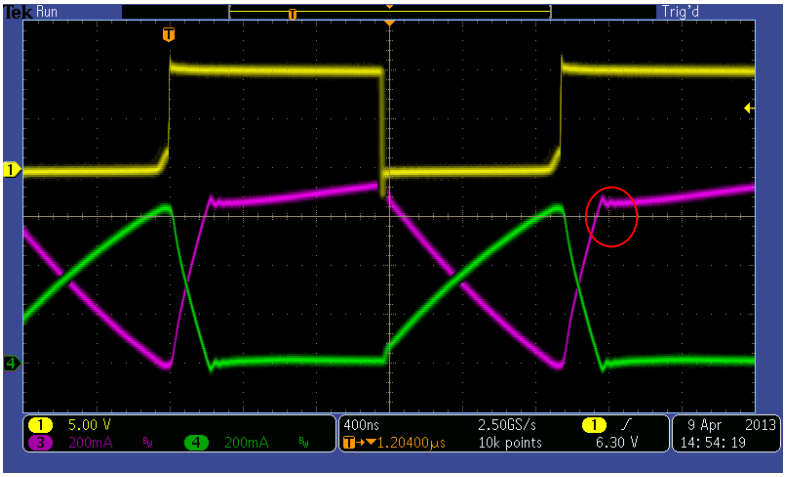

Figure 4: Primary switch node voltage (yellow). The section circled in red indicates DCM.

V_{IN} = 10,0 V, V_{O1} = 5,0 V, V_{O2} ≈ 3,0 V, I_{O1} = 500 mA, I_{O2} = 200 mA

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If the desired secondary load current $I_{O2\text{-}MAX}$ is higher than the lower of these two limits, there are several remedies:

1. Current ripple can be reduced by increasing the inductance, increasing the switching frequency, or both. This helps with both types of limit.
2. For current limit: a different control IC with a higher current limit threshold or a controller with external power MOSFETs and an adjustable threshold can be used.
3. For DCM limit: switching to a synchronous buck regulator that allows current in the inductor to reverse polarity and flow below zero allows the converter to maintain an average voltage of V_{OUT1} across the windings of the 1:1 inductor even when I_{O1} = zero. Several semiconductor companies have released small, cost-effective synchronous buck regulators targeted towards this application.

There is also a minimum current that the secondary output must supply in order to prevent V_{OUT2} from increasing at light or no-load conditions. The cause of this increase is a gradual transfer of energy to the secondary output capacitors from the energy in the leakage inductance of the inductor. Measuring leakage inductance and attempting to calculate the minimum load is generally impractical, and for this example lab testing with a potentiometer proved quick and effective. To keep the absolute value of V_{OUT2} below 5,5 V a maximum resistance of 1,1 kΩ is needed, and in the BOM a 1 kΩ resistor is used.

8. Accuracy of the Secondary Output Voltage

One disadvantage of using coupled inductors to generate secondary outputs is that only the primary output voltage is regulated by the feedback loop. Depending upon the tolerance of the reference voltage and of the feedback divider resistors, the main output V_{OUT1} enjoys a typical tolerance of ±1% to ±4% of the average V_{OUT1} value. V_{OUT2} is unregulated, however, and will shift with changes in input voltage and duty cycle. V_{OUT2} also shows a greater shift than V_{OUT1} with respect to the load currents of both the primary and the secondary. This is due to the voltage drops across the diodes and across the DC resistance (DCR) of the inductor windings and the PCB traces. Figure 5 shows a 1:1 inductor treated as an ideal transformer with a coupling efficient of 1, driven by a voltage equal to V_{OUT1} on the primary. By reflecting the voltage drops from the primary to the secondary it can be seen that V_{OUT2} is directly proportional to I_{O1} and is inversely proportional to I_{O2}.

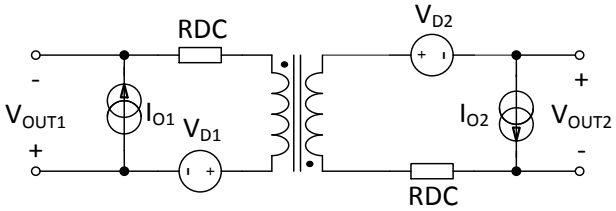

Figure 5: Primary and secondary voltage drops affect V_{OUT2}

The first-order equation governing V_{OUT2} is then:

$$V_{OUT2} = V_{OUT1} + I_{O1} \times DCR + V_{D1} - I_{O2} \times DCR - V_{D2} \quad \textbf{EQ.11}$$

In most design guides the forward voltage of a Schottky diode is assumed to be 0,5 V, however if V_{OUT2} is to be predicted with any accuracy the datasheets of the Schottkys used must be consulted or, better yet, the actual voltage drop measured. In practice the tolerance is also affected by the coupling coefficient between the two windings, and the effort of predicting V_{OUT2} to an accuracy of less than ±10 % is likely wasted, especially when the effect of load transients on either V_{OUT1} or V_{OUT2} are considered. For this example, even if the converter were sitting at just the right operating point to make the positive and negative terms of EQ.11 cancel, any load transient Δi would cause a shift of Δl * DCR. In conclusion, using V_{OUT2} without a linear

regulator is only practical for loads that have few or no load transients and that can tolerate a fairly wide range.

Table 1 shows the tolerance of V_{OUT2} for this example over various load and line conditions:

VIN (V)	I_{O1} (mA)	I_{O2} (mA)	V_{OUT2} (V)	V_{IN} (V)	I_{O1} (mA)	I_{O2} (mA)	V_{OUT2} (V)	V_{IN} (V)	I_{O1} (mA)	I_{O2} (mA)	V_{OUT2} (V)
10.0	50	25	4.65	12.0	50	25	4.84	14.0	50	25	4.89
10.0	100	25	4.95	12.0	100	25	5.02	14.0	100	25	5.05
10.0	200	25	5.03	12.0	200	25	5.13	14.0	200	25	5.16
10.0	500	25	5.25	12.0	500	25	5.37	14.0	500	25	5.41
10.0	50	50	3.55	12.0	50	50	4.14	14.0	50	50	4.41
10.0	100	50	4.51	12.0	100	50	4.74	14.0	100	50	4.85
10.0	200	50	4.75	12.0	200	50	4.89	14.0	200	50	4.98
10.0	500	50	4.93	12.0	500	50	5.12	14.0	500	50	5.23
10.0	50	100	1.67	12.0	50	100	2.38	14.0	50	100	2.93
10.0	100	100	3.07	12.0	100	100	3.79	14.0	100	100	4.15
10.0	200	100	4.00	12.0	200	100	4.40	14.0	200	100	4.58
10.0	500	100	4.23	12.0	500	100	4.62	14.0	500	100	4.81
10.0	200	200	2.22	12.0	200	200	3.02	14.0	200	200	3.50
10.0	500	200	3.28	12.0	500	200	3.69	14.0	500	200	4.02

Table 1: Secondary Voltage vs. Input Voltage, Primary Load and Secondary Load

9. Output Capacitors

Capacitors for smoothing the voltages at the converter outputs are selected with a similar philosophy as the inductor, but with a focus on maintaining a given maximum peak-to-peak ripple voltage instead of a ripple current. For the main output the ripple voltage is a function of the output capacitor´s impedance at the switching frequency and the peak-peak ripple current. The following equations assume that half of the impedance is due to the capacitive reactance, and half comes from the equivalent series resistance (ESR):

$$C_{O1-MIN} = \frac{\Delta i_P}{\Delta v_{O1} \times f_{SW} \times 4} = \frac{0{,}55A}{60mV \times 500kHz \times 4} = 4{,}55\mu F \quad \textbf{EQ.12}$$

$$ESR1_{MAX} = \frac{\Delta v_{O1}}{2 \times \Delta i_P} = \frac{60mV}{2 \times 0{,}55A} = 55m\Omega \quad \textbf{EQ.13}$$

For this example, a solid tantalum capacitor with 220 µF and ESR of 40 mΩ meets both requirements and provides much extra capacitance for responding to load transients. As a general practice, any time tantalum, aluminum or other high-ESR type capacitors are used at a switching converter´s input or output a 100 nF multi-layer ceramic capacitor (MLCC) placed in parallel will help reduce high frequency noise.

The secondary output requires that C_{O2} both filter and hold up V_{OUT2} while the control FET is on. This requires higher capacitance and a higher RMS current rating for an output of the same power. Fortunately V_{OUT2} only delivers a maximum of 200 mA. Minimum capacitance and maximum ESR are determined as follows:

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$$C_{O2-MIN} = \frac{I_{S-AVG} \times D_{MAX}}{\Delta v_{O2} \times f_{SW}} = \frac{0{,}42A \times 0{,}52}{60mV \times 500kHz} = 7{,}33\mu F \quad \textbf{EQ.14}$$

$$ESR2_{MAX} = \frac{\Delta v_{O2}}{I_{A-AVG}} = \frac{60mV}{0{,}42A} = 143m\Omega \quad \textbf{EQ.15}$$

Here it is important to calculate the RMS current as well:

$$I_{CO2-RMS} = I_{O2-MAX}\sqrt{\frac{D_{MAX}}{1-D_{MAX}}} = 0{,}2A\sqrt{\frac{0{,}52}{0{,}38}} = 0{,}18A_{RMS} \quad \textbf{EQ.16}$$

Tantalum and aluminum capacitors are possibilities, but in the face of heavy RMS current, MLCCs are the best choice. For this example a 22 µF device rated at 10V with X5R dielectric and 1210 case size will be used. The ESR is approximately 3 mΩ and the RMS current rating is about 3 A. One important consideration for MLCCs is their loss of capacitance under a DC voltage bias. This particular capacitor drops to about 16 µF when used at 5 VDC.

10. Input Capacitors

Input ripple voltage is often overlooked, but plays a vital role in conducted EMI. Input capacitors to buck regulators must withstand a discontinuous, heavy RMS current because they supply most of the AC current to the converter when the control FET is on. As with the secondary output capacitors, after minimum capacitance and maximum ESR have been selected, the capacitor or capacitors chosen must be evaluated for their RMS current ratings.

$$C_{IN-MIN} = (I_{O1-MAX} + I_{O2-MAX})\frac{D_{MAX}(1-D_{MAX})}{\Delta v_{IN-MAX} \times f_{SW}} = 0{,}7A\frac{0{,}52 \times 0{,}48}{0{,}2V \times 500kHz} = 1{,}75\mu F \quad \textbf{EQ.17}$$

$$I_{IN-PK} = \frac{P_{O-MAX}}{V_{IN-MIN} \times \eta} + \frac{\Delta i_P}{2} = \frac{3{,}5W}{10V \times 0{,}9} + \frac{0{,}55A}{2} = 1{,}02A \quad \textbf{EQ.18}$$

$$ESR_{IN-MAX} = \frac{\Delta v_{IN}}{I_{IN-PK}} = \frac{200mV}{1{,}02A} = 197m\Omega \quad \textbf{EQ.19}$$

The RMS current through the input capacitor is calculated as:

$$I_{CIN-RMS} = (I_{O1-MAX} + I_{O2-MAX})\sqrt{D_{MAX}(1-D_{MAX})} = 0{,}7A\sqrt{0{,}52 \times 0{,}46} = 0{,}35A_{RMS} \quad \textbf{EQ.20}$$

MLCCs are again the best choice due to their low ESR and high RMS current ratings. Here, a 25 V rated 10 µF device with X5R dielectric will be used. When biased at 14 V, the actual capacitance is approximately 7 µF.

11. Diodes

The recirculating diode for the main output (D1) and the output diode for the secondary (D2) are selected by calculating the average current carried and multiplying by the forward voltage to determine the power dissipation. The diode package is then selected based upon control of the temperature. Schottky diodes are

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preferred whenever they are available for their low forward voltage and near-zero reverse recovery charge, two features which combine to make them more efficient and less electrically noisy than PN diodes. For safety and margin when dealing with noise and transients, the reverse blocking voltage of the diodes should be selected at least 20% above the highest voltage in the system, which is V_{IN-MAX} for bucks and coupled bucks. 20% above 14 V is 16,8 V, hence 20 V or higher rated diodes will be used. Power dissipation is determined by the following equations:

$$P_{D1-MAX} = I_{O1-MAX} \times V_{D1}(1 - D_{MIN}) = 0{,}5A \times 0{,}5V(1 - 0{,}38) = 0{,}16W \quad \textbf{EQ.21}$$

$$P_{D2-MAX} = I_{O2-MAX} \times V_{D2} = 0{,}2A \times 0{,}5V = 0{,}1W \quad \textbf{EQ.22}$$

The industry standard SMA package with a typical thermal resistance of 95ºC/W is a cost-effective choice, and 20V rated devices are available from many different manufacturers.

12. Control Loop Compensation

Peak Current Mode control (PCM) is a good choice for controlling a buck using coupled inductors for several reasons. When properly designed this control method simplifies the design of the compensation of the error amplifier. As the name implies, PCM also controls peak current in the inductor (in this case in the primary winding) naturally and on a cycle-by-cycle basis. Adding a second winding and a second load to a buck converter changes the control-to-output transfer function of the power stage, comprised of the duty cycle modulator and the output filter. The basic goal of compensating the control loop stays the same, however. This is provide a high gain at DC (for best tolerance of the main output voltage), a high bandwidth (for fast response to load transients) and a high phase margin (for stable response to load and line transients.) There are many design philosophies for compensating control loops, and this application note will focus on a basic method that provides a conservative design that is very stable.

13. Defining the Power Stage

The inputs that are needed to develop a linear, small-signal model of the power stage of a 1:1 coupled buck regulator are as listed along with their values for this design example:

V_{IN-MIN} = 10 V **V_{OUT}** = 5,0 V **I_O** = I_{O1-MAX} + I_{O2-MAX} = 0,5 A + 0,2 A = 0,7 A **f_{SW}** = 500 kHz **L1** = 47 µH,

Power Stage Resistance, **R_L** = R_{DSON} of control MOSFET + DCR per winding of L1 = 200 + 600 = 800 mΩ

Total Output Capacitance, **C_O** = C_{O1} + C_{O2} = 220 µF + 16 µF = 236 µF

ESR of Output Capacitors, **R_C** = 40 mΩ Current Sense Resistance, **R_{SN}** = 167 mΩ

Current Sense Gain, **G_I** = 1 Reference Voltage, **V_{FB}** = 0,8 V Maximum Duty Cycle, **D_{MAX}** = 0,52

Load Resistance, **R_O** = V_{OUT} / I_O Slope Compensation Ramp, **V_M** = 0,417 V

The slope compensation ramp is used to correct for the error between the current at the point in time when it is sensed (at its peak) and the average value of that current. Without this additional slope, PCM switching converters exhibit a sub-harmonic oscillation for duty cycles of 50 % and above. Because the inductor ripple current is higher in a coupled buck than in a normal buck, a higher slope compensation ramp is needed.

Very few buck control ICs allow this ramp to be adjusted, hence it is important to evaluate the ideal slope compensation ramp to foresee any possible problems.

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For PCM the ideal compensation ramp is equal to the slope of the current during the off-time of the control FET. For simplicity it is assumed that the waveform is a triangle wave, but having the same peak-peak value as the actual trapezoid wave of Δi_P. The ideal compensation slope is then:

$$V_{SL-IDEAL} = \Delta i_P \times R_{SN} \times G_I = 0{,}55A \times 0{,}167\Omega \times 1 = 0{,}092V \quad \textbf{EQ.23}$$

The fixed ramp of 0,417 V used in the TPS54160 is higher than the ideal ramp, eliminating the danger of sub harmonic oscillation in this example. It should be noted that V_M cannot be made too high without consequences – if its value is far greater than the actual sensed slope, the converter becomes more of a voltage mode type and requires more careful compensation around the error amplifier to ensure an adequate phase margin.

$L1_{EFF}$ is used to correct for the difference between the slope of the triangular waveform of inductor current in a standard buck and the trapezoidal waveform of the inductor current in a coupled buck.

$$L1_{EFF} = \frac{V_{IN-MIN} - V_{OUT}}{\Delta i_P \times f_{SW}} \times D_{MAX} = \frac{10V - 5V}{0{,}55A \times 500kHz} \times 0{,}52 = 9{,}45\mu H \quad \textbf{EQ.24}$$

A_{FB} is the gain reduction that comes from the output divider resistors. K_M is the modulator gain, representing the balance between the sensed current slope (the first term in the denominator) and the compensation slope (second term in the denominator.)

$$A_{FB} = 20 \times \log\left(\frac{V_{FB}}{V_{OUT}}\right) = -15{,}9dB \quad \textbf{EQ.25}$$

$$K_M = \frac{1}{(0{,}5 - D_{MAX})R_{SN}\frac{1}{L1_{EFF} \times f_{SW}} + \frac{V_M}{V_{IN-MIN}}} = 24{,}6\frac{V}{V} \quad \textbf{EQ.26}$$

The DC gain of the power stage A_{PS} can be defined as follows:

$$A_{PS} = \frac{K_M \times R_O}{R_O + R_L + R_{SN} + K_M \times R_{SN} \times G_I} = 14{,}3dB \quad \textbf{EQ.27}$$

The frequency-dependent terms of the power stage are the load pole ω_C, the ESR zero ω_Z, and the double-pole derived from the sampling function of the inductor current with corner frequency ω_L.

$$\omega_C = \frac{1}{C_O}\left(\frac{1}{R_O} + \frac{1}{K_M R_{SN} G_I}\right) = 1{,}63\frac{krad}{s} \quad \textbf{EQ.28} \qquad \omega_Z = \frac{1}{R_C C_O} = 106\frac{krad}{s} \quad \textbf{EQ.29}$$

$$\omega_L = \frac{\frac{R_O R_C}{R_O + R_C} + R_L + R_{SN} + K_M R_{SN} G_I}{L1_{EFF}} = 534\frac{krad}{s} \quad \textbf{EQ.30}$$

The control-to-output transfer function can now be written in the LaPlace domain:

$$G_{PS}(s) = A_{PS}\frac{1 + \frac{s}{\omega_Z}}{\left(1 + \frac{s}{\omega_C}\right)\left(1 + \frac{s}{\omega_L} + \frac{s^2}{(\pi \times f_{SW})^2}\right)} \quad \textbf{EQ.31}$$

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The frequencies in Hertz of the poles and zero are calculated by dividing each in term in radians/sec by (2π):

$$f_C = \frac{\omega_C}{2\pi} = 260Hz \qquad f_Z = \frac{\omega_Z}{2\pi} = 17kHz \qquad f_L = \frac{\omega_L}{2\pi} = 85kHz$$

Plotting gain and phase graphically provides an intuitive way to place the gain and phase response needed for the error amplifier. Figure 6 shows the gain of $G_{PS}(s)$:

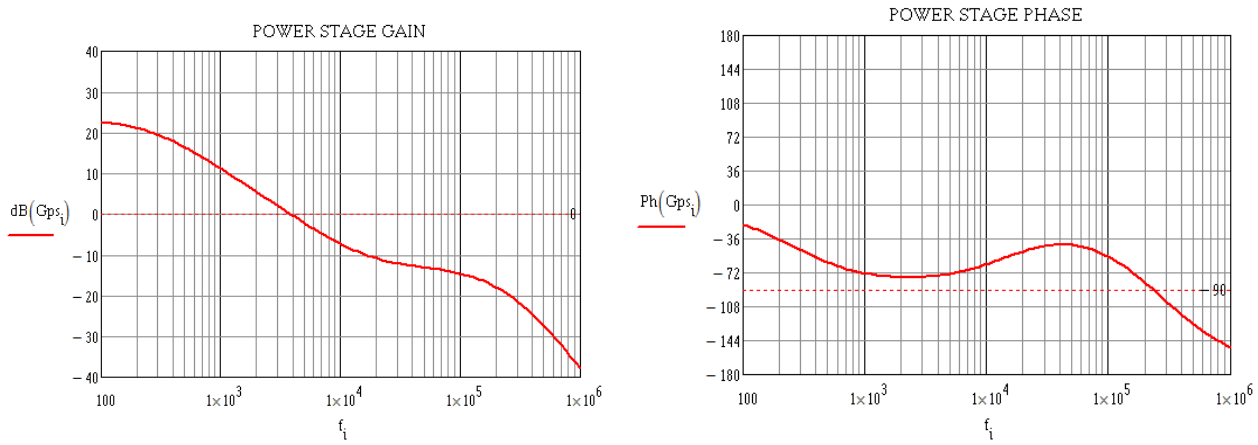

Figure 6: Power Stage Gain and Phase

From a graphical perspective, the goal of error amplifier compensation is to create a complete control loop gain that starts at a high level and rolls off at a slope of -20 dB/decade. The bandwidth or "crossover frequency" is defined as the point where the overall loop gain equals 0 dB, and in general bandwidth is made as high as possible while still maintaining a high phase margin. Phase margin turn is defined as the difference between the phase of the loop when gain equals zero dB and -360 º, the point at which the negative feedback becomes positive and implies an unstable control loop. (In practice the result is usually an unstable duty cycle and fluctuations of the output voltage.) A minimum phase margin of 45 º will ensure a transient response with little or no overshoot or oscillation while still allowing the bandwidth to be as much as 1/5th of the switching frequency. In theory the bandwidth could be as much as 1/2 of the switching frequency, but in practice 1/5th is a good upper limit.

In this example the compensation will be Type II, consisting of a pole at 0 Hz to ensure high DC gain at low frequencies, one pole whose frequency can be set arbitrarily and a zero whose frequency can also be set as desired. A good starting point is to set the compensation zero frequency f_{Z1} equal to the load pole f_C and to set the compensation pole frequency f_{P1} equal to the ESR zero frequency f_Z. The compensator pole and zero effectively cancel the power stage zero and pole, leaving only the pole at the origin, and in this way the high gain and continuous -20 dB/decade slope is maintained up until the sampling double pole frequency.

The remaining variable to be determined is the gain of the compensation between f_{Z1} and f_{P1}, often called the "mid-band gain". A good way to start is to set the overall control loop to cross 0 dB and define the bandwidth in this area of flat gain. This can be done by finding the gain of the power stage at the desired crossover frequency and then setting the gain of compensation to be equal in magnitude but opposite in sign, thus forcing the overall bandwidth to be zero at that point.

The TPS54160 uses a transconductance error amplifier with a gain of 97 µS along with two external capacitors and one external resistor to set the poles, zero, and mid-band gain. Figure 7 shows the error amplifier and the external components:

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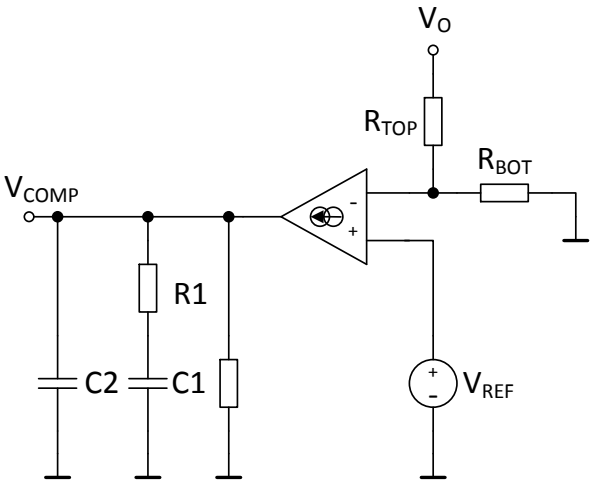

Figure 7: Transconductance Error Amplifier

The transconductance of the error amplifier can be read from the datasheet of the control IC, and for the TPS54160 this is g_M = 97 µS. The mid-band gain, pole and zero frequencies are as follows:

$$A_{MID} = g_M \times R1 \quad \textbf{EQ.32} \qquad f_{Z1} = \frac{1}{2\pi \times R1 \times C1} \quad \textbf{EQ.33} \qquad f_{P1} = \frac{1}{2\pi \times R1 \times C2} \quad \textbf{EQ.34}$$

Referring to Figure 6, the gain of $G_{PS}(S)$ at a conservative 1/10th of the switching frequency, or 50 kHz, is around -14 dB. Here there is one detail that is sometimes overlooked – the gain reduction from the feedback divider resistors, A_{FB}, defined in EQ.25. This term can be summed with the power stage or with the error amplifier – it makes no difference once the loop is closed. This example assumes that A_{FB} is part of the error amplifier, and since it is a DC gain, it affects the mid-band gain:

$$A_{FB} = 20\log\left(\frac{0{,}8V}{5V}\right) = -15{,}9dB \qquad A_{MID} = 10^{\frac{A_{0dB}\times(-1)+A_{FB}}{20}} = 10^{\frac{-14\times(-1)+15{,}9}{20}} = 31{,}3\frac{V}{V} \quad \textbf{EQ.35}$$

Now that mid-band gain has been calculated, R1, C1 and C2 can be calculated:

$$R1 = \frac{31{,}3V/V}{97\mu S} = 322k\Omega \qquad C1 = \frac{1}{2\pi \times 322k\Omega \times 260Hz} = 1{,}9nF$$

$$C2 = \frac{1}{2\pi \times 322k\Omega \times 17kHz} = 29\,pF$$

The closest 1 % resistor value is 316 kΩ and the closest 10 % capacitor values are 1,8 nF and 27 pF, respectively. These are substituted into the compensation transfer function:

$$G_{EA}(s) = g_M A_{FB} \frac{s \times R1 \times C1 + 1}{s(s \times R1 \times C1 \times C2 + C1 + C2)} \quad \textbf{EQ.36}$$

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Figure 8 shows the gain and phase of the error amplifier:

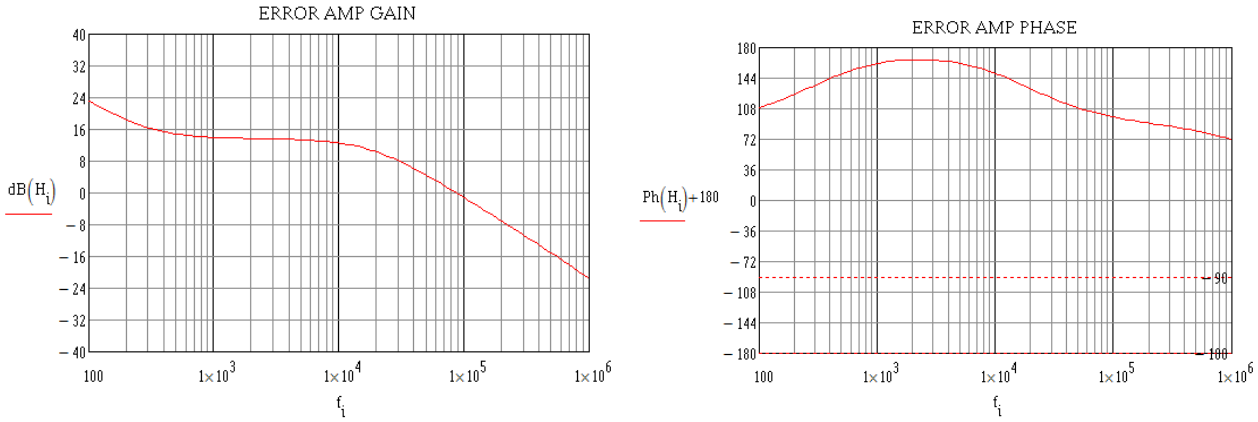

Figure 8: Error Amp Gain and Phase

The final step is to close the loop by multiplying the power stage and error amplifier transfer functions together. The final gain plot shows bandwidth and the final phase plot shows the phase margin:

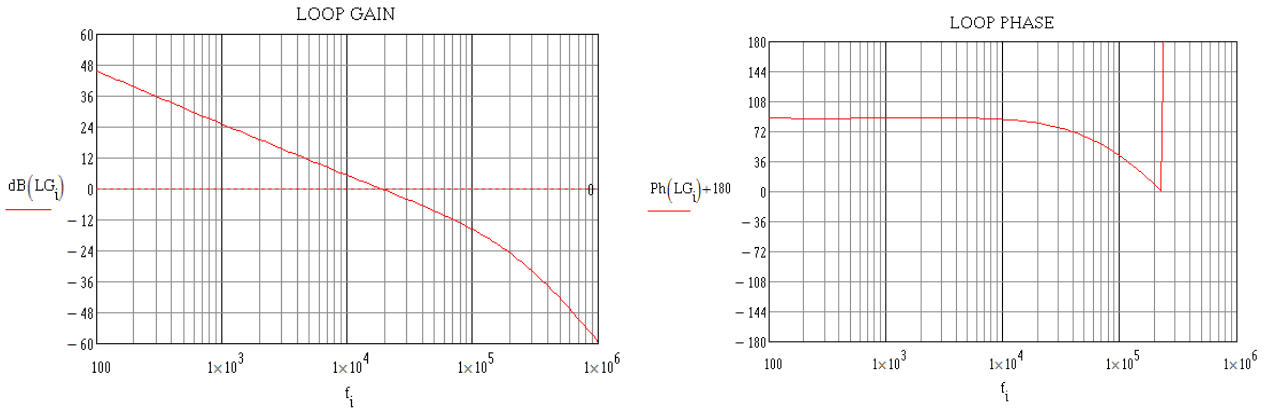

Figure 9: Overall Control Loop Gain and Phase

The actual bandwidth is 20 kHz and the phase margin 79 º, indicating a somewhat slow but very stable control loop. The reason bandwidth and phase margin don´t match the predictions perfectly is the relatively low frequency of the compensation pole. This is typical for converters using output capacitors with high ESR such as aluminum electrolytic and tantalum. The frequency of the compensation pole can be increased up to ½ of the switching frequency if desired. In fact, for converters with purely ceramic output capacitors the ESR zero frequency is typically in the MHz range, and in such cases ½ of the switching frequency is the recommended compensation pole frequency. Increasing the mid-band gain and/or increasing the compensation pole frequency will increase the control loop bandwidth, but will also decrease the phase margin. Several iterations of incrementing the bandwidth and monitoring the phase margin can be performed until phase margin has dropped to 45 º, at which point the maximum recommended bandwidth is reached.

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14. L-C Input Filter with Damping

Buck converters, buck-boost converters and flyback converters are the three principal topologies that draw a discontinuous current from the input source. Even with good quality input capacitors to supply the heavy AC current, the source will supply some current at AC, and the result is conducted electromagnetic interference (EMI) on the input lines. The longer the leads, PCB traces and wiring harnesses that connect these high ripple DC-DC converters to their input sources, the more likely that this conducted EMI also becomes radiated EMI owing to the unwanted antenna behavior of the leads. An input L-C filter placed close to the DC-DC converter is a good way to reduce conducted EMI, and by filtering before the noise can "contaminate" the input leads radiated EMI is reduced as well.

Not every laboratory has access to dedicated equipment for measuring and testing conducted EMI, let alone the special antennas and anechoic chambers needed for radiated EMI. The following procedure is based upon correlation of time-domain current waveforms that can be predicted and measured with a common oscilloscope to differential-mode conducted noise in the frequency domain.

15. Estimating Noise Amplitude

The following equation can be used to estimate the amplitude of the first harmonic of the differential mode conducted noise based upon the input current waveform:

$$A_{1ST} = 20 \times \log\left(\frac{\frac{I_{IN-AVG}}{\pi^2 C_{IN} f_{SW}} \sin(\pi \times D_{MAX})}{1\mu V}\right) \quad \textbf{EQ.37}$$

Figure 10 shows the input current of the example circuit during maximum load and minimum input voltage – the worst-case for EMI.

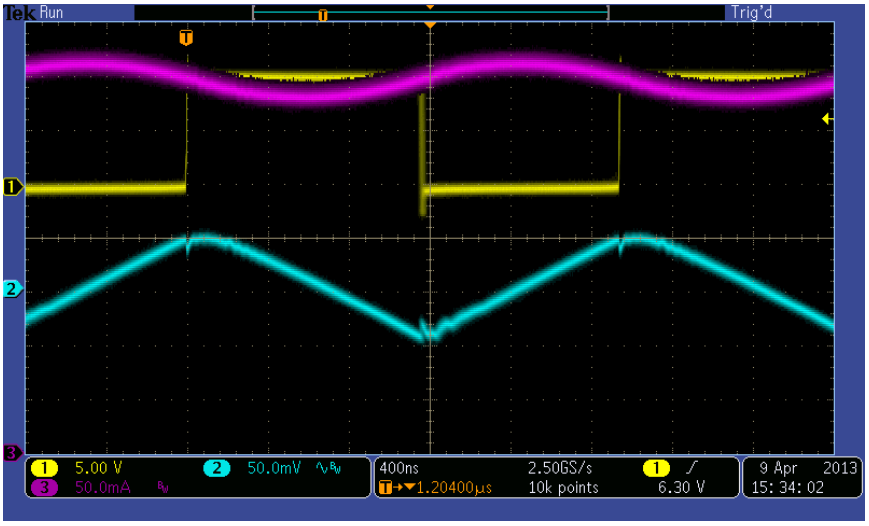

Figure 10: Primary switch node (yellow), Δv_{IN} (AC-coupled, blue), I_{IN} (pink)

V_{IN} = 10V, I_{O1} = 500 mA, I_{O2} = 180 mA

Average input current, or the average height of the pedestals of trapezoid wave input current can be calculated as:

$$I_{IN-AVG} = \frac{I_{IN}}{D_{MAX}} \quad \textbf{EQ.38} \qquad I_{IN} = \frac{V_{OUT}(I_{O1}+I_{O2})}{V_{IN-MIN}\times\eta} = \frac{5V(0{,}5A+0{,}2A)}{10V\times 0{,}9} = 0{,}39A \quad \textbf{EQ.39}$$

Maximum duty cycle was defined in EQ.1 as 0,52, and the average current is then 0,39 / 0,52 = 0,75 A. The total input capacitance C_{IN} is 7 µF. The estimated noise of the first harmonic is:

$$A_{1ST} = 20\times\log\left(\frac{\frac{0{,}75A}{\pi^2\times 7\mu F\times 500kHz}\sin(\pi\times 0{,}52)}{1\mu V}\right) = 86{,}6\ dB\mu V$$

The limit for average common mode noise in many standards for conducted EMC, e.g.: IEC55022 in the range of 500 kHz is 46 dBµV, hence the attenuation needed is equal to the noise A_{1ST} minus this limit. For this example the required attenuation is then A_{TT} = 86,6 – 46 = 41 dBµV.

16. Selecting L and C

Either the inductance or the capacitance of the input filter must be chosen arbitrarily, and for this example it is the inductance that will be chosen first. Values of inductance between 1 and 10 µH provide a good compromise between size, cost, and the resulting resonant frequency of the input L-C filter. The RMS current rating of the inductor must be greater than the input current I_{IN}, and the peak current rating must be higher than the sum of the average current and one-half of the AC ripple:

$$I_{SAT-MIN} \geq I_{IN-PK} = I_{IN-AVG} + \frac{\Delta i_P}{2} = 0{,}75A + \frac{0{,}55A}{2} = 1{,}02A \quad \textbf{EQ.40}$$

The Würth Elektronik WE-TPC 2828 series 744 025 002 is a shielded 2,2 µH device in a small footprint (2,8 x 2,8 x 2,8 mm) with a DCR of 60 mΩ and current ratings of I_{RMS} = 1,8 A and I_{SAT} = 2,4 A that is well suited for this example. With inductance chosen, two equations exist for selecting the required capacitance. The first is based upon the resonant frequency of the filter, which should be kept to 1/10th of the switching frequency or less:

$$C_{F-MIN1} = \frac{C_{IN}}{C_{IN}\times L_F\left(\frac{2\pi f_{SW}}{10}\right)^2 - 1} = \frac{7\mu F}{7\mu F\times 2{,}2\mu H\left(\frac{2\pi\times 500kHz}{10}\right)^2 - 1} = 13{,}5\mu F \quad \textbf{EQ.41}$$

The result of EQ.41 may be negative – this would indicate that with the chosen inductor value it is not possible to attain a filter resonance frequency 10x lower than the switching frequency. The inductor value can be increased if desired, though this comes at a penalty of lower efficiency and/or a larger inductor due to the higher DCR and higher core losses that accompany higher inductance. Setting resonant frequency 10x below switching frequency is a guideline, not a hard limit.

The second equation is a hard limit, and it predicts the minimum capacitance needed to ensure that the voltage ripple at the input to the converter is below the limit set by A_{TT}:

$$C_{F-MIN2} = \frac{1}{L_F}\left(\frac{10^{\frac{A_{TT}}{40}}}{2\pi f_{SW}}\right)^2 = \frac{1}{2{,}2\mu H}\left(\frac{10^{\frac{41}{40}}}{2\pi \times 500kHz}\right)^2 = 5{,}0\mu F \quad \textbf{EQ.42}$$

The capacitor chosen should be greater than the larger of the two values given by $C_{F\text{-}MIN1}$ and $C_{F\text{-}MIN2}$, and multi-layer ceramic capacitors are the best choice. When using MLCCs the loss in capacitance due to a DC voltage bias must be taken into account. Depending upon the case size and voltage rating it would likely take two or more 10 µF capacitors in parallel to provide a true 14 µF or more of capacitance. Before selecting the final value for C_F, however, the damping of the input filter must be considered.

17. Filter Damping

Any time an L-C filter feeds into a switching regulator the potential exists for an oscillation (often called “ringing” or also “power supply interaction”) stemming from the output impedance of the filter and the input impedance of the switcher. Properly designed switchers maintain high power efficiency over a range of input voltage, and one effect of this is that as input voltage rises, input current decreases, and vice-versa. The result is effective negative input impedance. If $|-Z_{IN}|$ is less than or equal to Z_{OUT} of the L-C filter, the input line is likely to oscillate, a behavior that is never beneficial.

Even in the absence of an input inductor, the input leads have a parasitic inductance, and when switchers use purely MLCC input capacitors with their very low ESR the potential for oscillation is very real. In this example there is a discrete inductor whose inductance and DCR are both known. With these quantities a damping capacitor C_D can be selected to go in parallel with C_{IN}, shown in Figure 11.

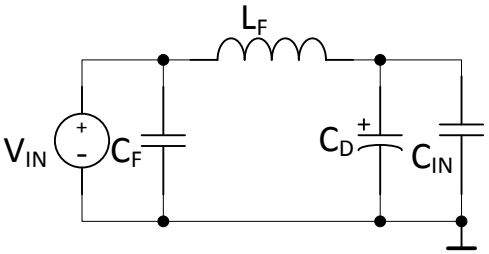

Figure 11: L-C filter with damping capacitor

Besides stopping any oscillations, C_D reduces the ripple voltage at the input, lowering the amplitude of A_{1ST} and A_{TT}, and in turn reducing the capacitance needed for C_F. The following two equations define the minimum capacitance and the minimum ESR needed for C_D to critically damp the filter formed by L_F and C_{IN}:

$$C_D \geq C_{IN} \times 4 = 7\mu F \times 4 = 28\mu F \quad \textbf{EQ.43}$$

$$ESR \geq \frac{1}{2}\sqrt{\frac{L_F}{C_{IN}}} - DCR = \frac{1}{2}\sqrt{\frac{2{,}2\mu H}{7\mu F}} - 0{,}06\Omega = 0{,}22\Omega \quad \textbf{EQ.44}$$

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A negative value for the ESR would indicate that the inductor DCR already provides enough damping resistance. The typical choice for C_D is an aluminum electrolytic capacitor. Surface mount aluminum capacitors rated to 16 V or 25 V with 33 µF are available at reasonable cost from many different manufacturers. What´s more, for damping the normally “bad” characteristic, high ESR, is actually helpful. A surface mount aluminum electrolytic capacitor rated at 25 V provides 33 µF with an ESR of 0,34 Ω in a compact 6,3 mm radius footprint, or Radial D8 Case.

18. Re-evaluate C_F

The total capacitance of C_{IN} is now equal to (7 µF + 33 µF), so another iteration of the filter capacitor design is needed. For simplicity the results will simply be stated: the final C_F value needed is 5,2 µF. Another 25 V rated, nominal 10 µF MLCC identical to C_{IN} will be used, and since the DC bias is the same, this capacitor will provide at least 7 µF of capacitance.

19. Conclusion

Using a coupled inductor can help derive a second output voltage without the cost of another complete switching power supply, but the tolerance of the secondary output voltage and the DCM threshold in the primary are difficult to predict with pure mathematical expressions. Successful 1:1 coupled buck designs should be lab tested thoroughly, over line, load and temperature. In most cases the secondary output voltage tolerance is too wide, line regulation too high and load regulation too high to be used directly. For all of these reasons a linear regulator is the recommended way to provide a well-regulated secondary output.

20. Graphs and Oscilloscope Captures

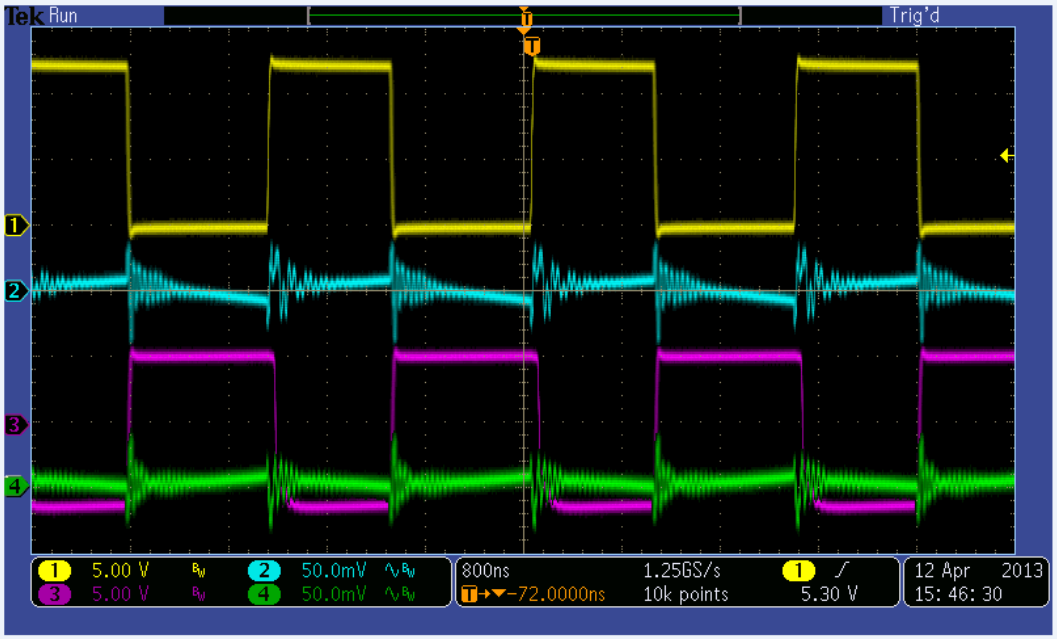

Figure 12: Steady State Waveforms. I_{O1} = 500 mA, I_{O2} = 100 mA
Ch.1 = Primary SW, Ch.2 = V_{OUT1} AC-coupled, Ch.3 = Secondary SW, Ch.4 = V_{OUT2} AC-coupled

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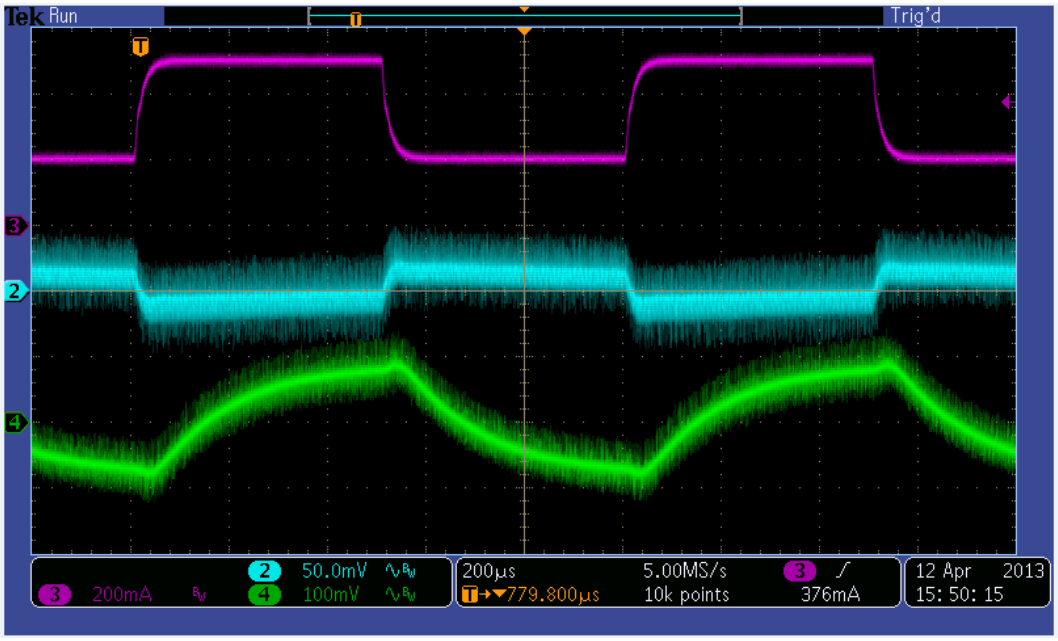

Figure 13: Load Transient on Primary. I_{O1} varies from 200 to 500 mA, I_{O2} = 100 mA
Ch.2 = V_{OUT1} AC-coupled, Ch.3 = I_{O1}, Ch.4 = V_{OUT2} AC-coupled

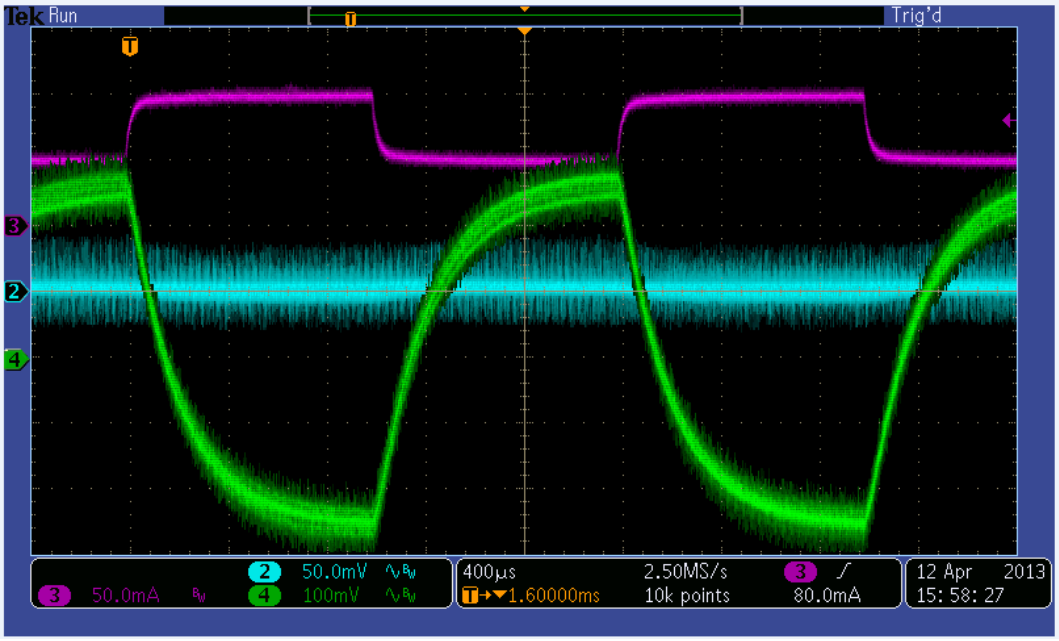

Figure 14: Load Transient on Secondary. I_{O1} = 500 mA, I_{O2} varies from 50 to 100 mA
Ch.2 = V_{OUT1} AC-coupled, Ch.3 = I_{O1}, Ch.4 = V_{OUT2} AC-coupled

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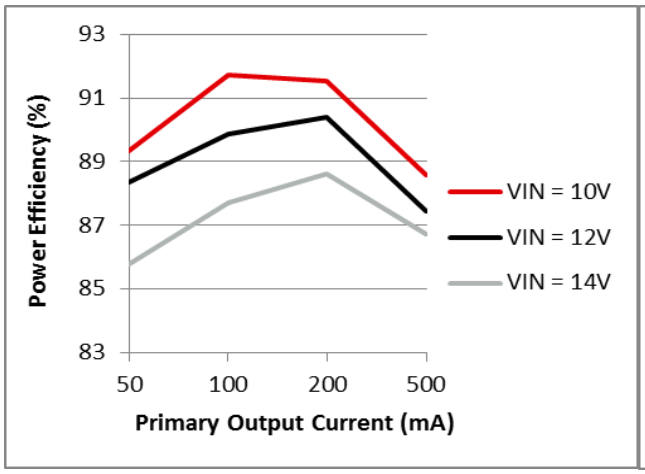
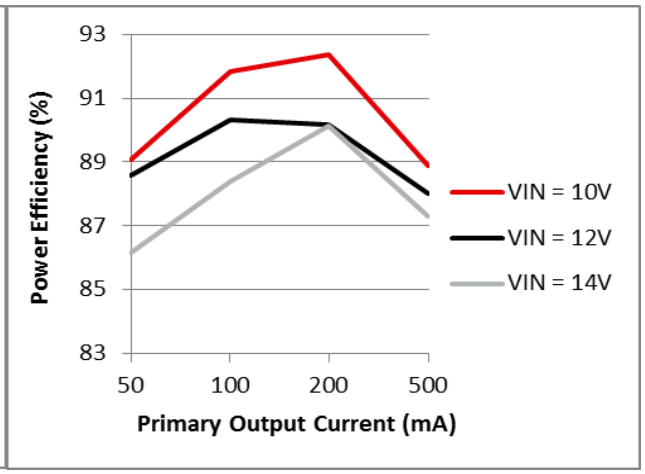
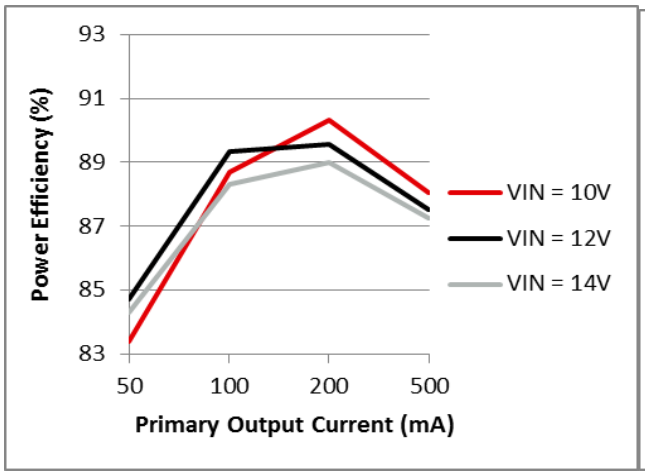


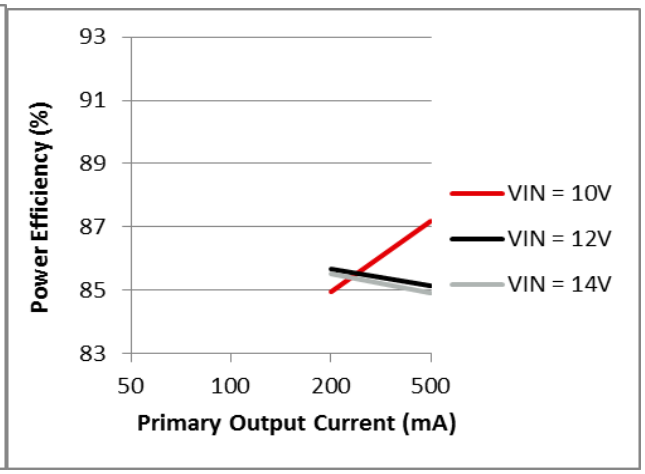
Power Efficiency, I_{O2} = 25 mA



Power Efficiency, I_{O2} = 50 mA

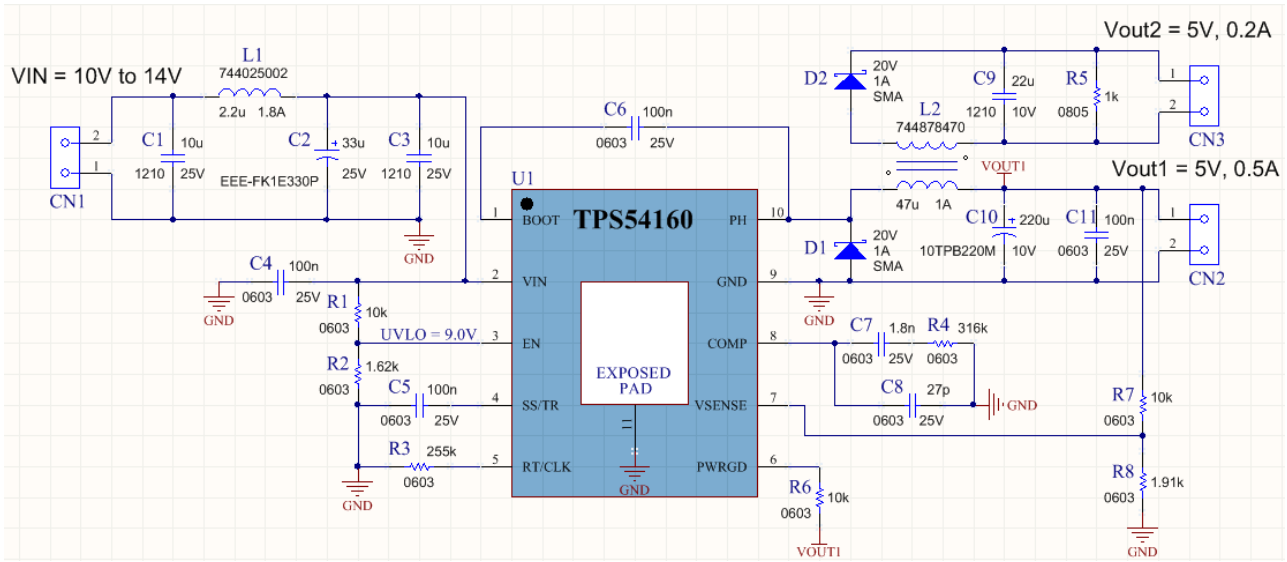


Power Efficiency, I_{O2} = 100 mA



Power Efficiency, I_{O2} = 200 mA

21. Complete Circuit Schematic



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22. Bill of Materials

Designator	Quantity	Component Type	Description	Package/Size	Part Number	Value1	Value2	Value3	Manufacturer
C10	1	Capacitor	SMT Polarized D Case	D-Case	10TPB220M	220u	10V	4mohm	SANYO
C2	1	Capacitor	SMT Polarized D8 Case	Radial D8	EEE-FK1E330P	33u	25V	0.34ohm	Panasonic
CN1, CN2, CN3	3	Terminal Block	3.81mm Wire to Board	7.62x7.4x8.5mm	691214310002	300Vrms	10A	3.81mm	Würth Elektronik
R1, R6, R7	3	Resistor	Thick Film	0603	CRCW06031002FK	10k	0.1W	75V	Vishay-Dale
R2	1	Resistor	Thick Film	0603	CRCW06031621FK	1.62k	0.1W	75V	Vishay-Dale
R3	1	Resistor	Thick Film	0603	CRCW06032553FK	255k	0.1W	75V	Vishay-Dale
R4	1	Resistor	Thick Film	0603	CRCW06033163FK	316k	0.1W	75V	Vishay-Dale
R5	1	Resistor	Thick Film	0805	CRCW08051001FK	1k	0.125W	150V	Vishay-Dale
R8	1	Resistor	Thick Film	0603	CRCW06031911FK	1.91k	0.1W	75V	Vishay-Dale
C1, C3	2	Capacitor	MLCC	1210	C3225X5R1E106M	10u	25V	X5R	TDK
C4, C5, C6, C11	4	Capacitor	MLCC	0603	C1608X7R1E104M	100n	25V	X7R	TDK
C7	1	Capacitor	MLCC	0603	C1608COG1H182J	1.8n	25V	X5R	TDK
C8	1	Capacitor	MLCC	0603	C1608COG1H270J	27p	25V	X5R	TDK
C9	1	Capacitor	MLCC	1210	C3225X5R1A226M	22u	10V	X5R	TDK
D1, D2	2	Schottky Diode	SMA (DO-214AC)	SMA	B120-13-F	20V	1A	0.5V	Diodes Inc
L1	1	Inductor	Shielded Drum Core	2.8x2.8x2.8mm	744025002	2.2u	1.8A	60mohm	Würth Elektronik
L2	1	Inductor	Shielded 1:1 Coupled	7.3x7.3x4mm	744878470	47u	1A	0.6ohm	Würth Elektronik
U1	1	IC	Non-sync Buck Regulator	eMSOP-10	TPS54160DGQ				Texas Instruments

APPLICATION NOTE

Designing Low-cost, Multiple Output DC-DC Converters

Using 1:1 Coupled Inductors with Buck Regulators

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USEFUL LINKS

Application Notes:	http://www.we-online.com/app-notes
Component Selector:	http://www.we-online.com/component-selector
Toolbox:	http://www.we-online.com/toolbox
Product Catalog:	http://katalog.we-online.de/en/

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